Towards European High Performance Computing Accelerators based on the RISC-V Open ISA

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Designing RISC-V-based Accelerators for next generation Computers (DRAC) is a 3.5-year project (2019-2023) funded by the ERDF Operational Program of Catalonia 2014-2020. DRAC will design, verify, implement and fabricate a high performance general purpose processor that will incorporate different accelerators based on the RISC-V technology, with specific applications in the field of post-quantum security, genomics and autonomous navigation. In this talk, we will provide an overview of the main achievements in the DRAC project, including the fabrication of Lagarto, the first RISC-V processor developed in Spain. Moreover, we will present multiple European initiatives to achieve European technological independence based on the RISC-V open instruction set architecture.